AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A decoder, comprising:

a feedback equalizer for receiving a modulated signal comprising a plurality of symbols, the plurality of symbols including a first symbol defined by a first number of chips; and

a subsymbol processor coupled to said feedback equalizer to generate a subsymbol waveform upon receipt of a second number of chips of the first symbol and before at least one of receiving, decoding, and deciding the first number of chips of the first symbol and to provide the subsymbol waveform to the feedback equalizer, the second number being less than the first number, said feedback equalizer to equalize the modulated signal using the subsymbol waveform.

2. (Original) The decoder of Claim 1, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

3. (Previously Presented) The decoder of Claim 1, said feedback equalizer further comprising:

a hard decision unit coupled to said equalizer for determining hard decision information associated with the modulated signal; and

a feedback filter coupled to said hard decision unit and said subsymbol processor to selectively equalize the modulated signal using one of the hard decision information and the subsymbol waveform.

4. (Currently Amended) A decoder, comprising:

a feedback equalizer for receiving a modulated signal comprising a plurality of symbols, the plurality of symbols including a first symbol defined by a first number of chips;

a subsymbol processor coupled to said feedback equalizer to generate a subsymbol waveform upon receipt of a second number of chips of the first symbol and provide the subsymbol waveform to the feedback equalizer, the second number being less than the first number, said feedback equalizer to equalize the modulated signal using the subsymbol waveform; ~~The decoder of Claim 1, wherein the symbol processor comprises:~~

a demodulation unit coupled to said feedback equalizer and comprising subsymbol decoding processing logic ~~capable of~~ for generating decoded subsymbol information upon ~~perceiving~~ receiving the second number of chips of the symbol; and

a remodulation unit coupled to said demodulation unit and said feedback equalizer, said remodulation unit generating a subsymbol waveform corresponding to the decoded subsymbol information.

5. (Currently Amended) The decoder of Claim 4, wherein said demodulation unit further comprises a symbol correlator coupled to said decoding processing logic to

correlate the ~~perceived~~ perceived received second number of chips against a subset of valid candidate symbols to obtain a best match candidate, said decoding processing logic generating the decoded subsymbol information based on the best match candidate.

6. (Original) The decoder of Claim 4, wherein said demodulation unit further comprises decision processing logic capable of deciding the symbol upon receipt of the first number of chips defining the symbol.

7. (Original) The decoder of Claim 6, wherein said decision processing logic comprises first and second demodulation pathways capable of deciding the symbol by at least one of first and second distinct modulation modes.

8. (Original) The decoder of Claim 7, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCIQ compliant with IEEE Standard 802.11b (1999) respectively.

9. (Original) The decoder of Claim 1, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

10-18. (Cancelled)

19. (Currently Amended) A transceiver, comprising:

a feedback equalizer ~~capable of of~~ for receiving a modulated signal, comprising a plurality of symbols, the plurality of symbols including a first symbol defined by a first number of chips; and

a subsymbol processor coupled to said feedback equalizer to generate a subsymbol waveform upon receipt of a second number of chips of the first symbol and before at least one of receiving, decoding, and deciding the first number of chips of the first symbol and to provide the subsymbol waveform to the feedback equalizer, the second number being less than the first number, said feedback equalizer to equalize the modulated signal using the subsymbol waveform.

20. (Original) The transceiver of Claim 19, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

21. (Original) The transceiver of Claim 19, said feedback equalizer comprising:

a hard decision unit coupled to said equalizer for determining hard decision information associated with the modulated signal; and

a feedback filter coupled to said hard decision unit and said symbol processor to selectively equalize the modulated signal using one of the hard decision information and the subsymbol waveform.

22. (Original) A transceiver, comprising:

a feedback equalizer ~~of~~ for receiving a modulated signal, comprising a plurality of symbols, the plurality of symbols including a first symbol defined by a first number of chips;

a subsymbol processor coupled to said feedback equalizer to generate a subsymbol waveform upon receipt of a second number of chips of the first symbol and provide the subsymbol waveform to the feedback equalizer, the second number being less than the first number, said feedback equalizer to equalize the modulated signal using the subsymbol waveform; ~~The transceiver of Claim 19, wherein the symbol processor comprises:~~

a demodulation unit coupled said feedback equalizer and comprising decoding processing logic capable of generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

a remodulation unit coupled to said demodulation unit and said feedback equalizer, said remodulation unit generating a subsymbol waveform corresponding to the decoded subsymbol information.

23. (Original) The transceiver of Claim 22, wherein said demodulation unit further comprises a symbol correlator coupled to said decoding processing logic to correlate the perceived second number of chips against a subset of valid candidate symbols to obtain a best match candidate, said decoding processing logic generating the decoded subsymbol information based on the best match candidate.

24. (Original) The transceiver of Claim 22, wherein said demodulation unit further comprises decision processing logic capable of deciding the symbol upon receipt of the first number of chips defining the symbol.

25. (Original) The transceiver of Claim 24, wherein said decision processing logic comprises first and second demodulation pathways capable of deciding the symbol by at least one of first and second distinct modulation modes.

26. (Original) The transceiver of Claim 25, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

27. (Original) The transceiver of Claim 19, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

28. (Original) The transceiver of Claim 19, further comprising RF and IF sections coupled to said feedback equalizer to provide the modulated signal to said feedback equalizer.

29. (Original) A base station comprising the transceiver of Claim 28.

30. (Original) A network card comprising the transceiver of Claim 28.

31. (Original) An information processing system, comprising the transceiver of Claim 19.

32. (Currently Amended) A decoding method for a modulated signal including a symbol defined by a first number of chips, comprising:

generating a subsymbol waveform upon receipt of a second number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the symbol, the second number being less than the first number; and

equalizing the modulated signal using the subsymbol waveform.

33. (Currently Amended) The method of Claim 32, wherein the subsymbol [[\]]\waveform waveform includes a third number of chips, the third number being less than or equal to the second number.

34. (Original) The method of Claim 32, further comprising:

determining hard decision information associated with the modulated signal; and

wherein said equalizing step comprises selectively equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

35. (Previously Presented) The method of Claim 32, wherein said generating step comprises:

generating decoded subsymbol information upon receiving the second number of chips of the symbol; and

generating a subsymbol waveform corresponding to the decoded subsymbol information.

36. (Currently Amended) A decoding method for a modulated signal including a symbol defined by a first number of chips, comprising:

generating a subsymbol waveform upon receipt of a second number of chips of the symbol, the second number being less than the first number, wherein said generating step comprises:

generating decoded subsymbol information upon receiving the second number of chips of the symbol; and

generating a subsymbol waveform corresponding to the decoded subsymbol information;

equalizing the modulated signal using the subsymbol waveform; and

~~The method of Claim 35, further comprising:~~

correlating the ~~perceived~~ received second number of chips against a subset of valid candidate symbols to obtain a best match candidate; and

wherein said decoded subsymbol generating step comprises generating the decoded subsymbol information based on the best match candidate.

37. (Original) The method of Claim 35, further comprising deciding the symbol upon receipt of the first number of chips defining the symbol.

38. (Original) The method of Claim 37, wherein said deciding step comprises deciding the symbol by at least one of first and second distinct modulation modes.

39. (Original) The method of Claim 38, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

40. (Original) The method of Claim 32, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

41. (Currently Amended) A computer program product, comprising computer readable program code causing an information processor to perform the following steps, comprising:

receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips;

generating a subsymbol waveform upon receipt of a second number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the symbol, the second number being less than the first number; and

equalizing the modulated signal using the subsymbol waveform.

42. (Original) The product of Claim 41, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

43. (Original) The product of Claim 41, further comprising:

computer readable program code causing the information processor to perform the step of determining hard decision information associated with the modulated signal; and

wherein said equalizing step comprises selectively equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

44. (Original) The product of Claim 41, wherein said generating step comprises:

generating decoded subsymbol symbol information upon perceiving the second number of chips of the symbol; and

generating a subsymbol waveform corresponding to the decoded subsymbol information.

45. (Currently Amended) A computer program product, comprising computer readable program code causing an information processor to perform the following steps, comprising:

receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips;

generating a subsymbol waveform upon receipt of a second number of chips of the symbol, the second number being less than the first number, wherein said generating step comprises:

generating decoded subsymbol symbol information upon perceiving the second number of chips of the symbol; and

generating a subsymbol waveform corresponding to the decoded subsymbol information;

equalizing the modulated signal using the subsymbol waveform; and

~~The product of Claim 44, further comprising:~~

~~computer readable program code causing the information processor to perform the step of~~ correlating the perceived second number of chips against a subset of valid candidate symbols to obtain a best match candidate; and

wherein said decoded subsymbol symbol generating step comprises generating the decoded subsymbol information based on the best match candidate.

46. (Original) The product of Claim 44, further comprising computer readable program code causing the information processor to perform the step of deciding the symbol upon receipt of the first number of chips defining the symbol.

47. (Original) The product of Claim 46, wherein said deciding step comprises deciding the symbol by at least one of first and second distinct modulation modes.

48. (Original) The product of Claim 47, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

49. (Original) The product of Claim 41, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

50. (Currently Amended) An information processing system including an information processor coupled to memory, the memory comprising computer readable program code causing the information processor to perform the following operations, comprising:

receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips;

generating a subsymbol waveform upon receipt of a second number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the symbol, the second number being less than the first number; and

equalizing the modulated signal using the subsymbol waveform.

51. (Original) The system of Claim 50, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

52. (Original) The system of Claim 50, wherein the memory further comprises computer readable program code causing the information processor to perform the step of determining hard decision information associated with the modulated signal; and

wherein said equalizing step comprises selectively equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

53. (Original) The system of Claim 50, wherein said generating step comprises:

generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

generating a subsymbol waveform corresponding to the decoded subsymbol information.

54. (Currently Amended) An information processing system including an information processor coupled to memory, the memory comprising computer readable program code causing the information processor to perform the following operations, comprising:

receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips;

generating a subsymbol waveform upon receipt of a second number of chips of the symbol, the second number being less than the first number, wherein said generating step comprises:

generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

generating a subsymbol waveform corresponding to the decoded subsymbol information;

equalizing the modulated signal using the subsymbol waveform; and

~~The system of Claim 53, wherein the memory further comprises computer readable program code causing the information processor to perform the step of~~ correlating the perceived second number of chips against a subset of valid candidate symbols to obtain a best match candidate; and

wherein said decoded subsymbol generating step comprises generating the decoded subsymbol information based on the best match candidate.

55. (Original) The system of Claim 53, wherein the memory further comprises computer readable program code causing the information processor to perform the step of deciding the symbol upon receipt of the first number of chips defining the symbol.

56. (Original) The system of Claim 55, wherein said deciding step comprises deciding the symbol by at least one of first and second distinct modulation modes.

57. (Original) The system of Claim 56, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

58. (Currently Amended) The system of Claim [[41]] 4150, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

59. (Currently Amended) A decoder, comprising:

a feedback equalizer capable of receiving a modulated signal, the modulated signal including a plurality of symbols a Barker encoded symbol defined by a first number of chips; and

a symbol processor coupled to said feedback equalizer to generate a decoded waveform upon receipt of a second number of chips of the symbol less than the first number and before at least one of receiving, decoding, and deciding the first number of chips of the symbol, and to provide the decoded waveform to the feedback equalizer, said feedback equalizer to equalize the modulated signal using the decoded waveform.

60. (Original) The decoder of Claim 59, wherein the modulated signal further includes a non-Barker encoded symbol defined by a second number of chips.

61. (Original) The decoder of Claim 60, wherein the non-Barker encode symbol comprises a CCK encoded symbol; and

wherein the Barker encoded and CCK encoded symbols are modulated in compliance with IEEE Standard 802.11b (1999).

62. (Original) A transceiver, comprising the decoder of Claim 61.

63. (Original) A base station, comprising the transceiver of Claim 62.

64. (Original) A network card comprising the transceiver of Claim 62.

65. (Original) An information processing system comprising the transceiver of Claim 62.

66-68. (Cancelled)

69. (Currently Amended) A decoding method for a modulated signal including a plurality of symbols including a Barker encoded symbol defined by a first number of chips, comprising:

generating a decoded waveform upon receipt of a second number of chips less than the first number of chips of the Barker encoded symbol and before at least one of receiving, decoding, and deciding the first number of chips of the Barker encoded symbol; and

equalizing the modulated signal using the decoded waveform.

70. (Original) The method of Claim 69, wherein the modulated signal further includes a non-Barker encoded symbol defined by a second number of chips.

71. (Original) The method of Claim 70, wherein the non-Barker encode symbol comprises a CCK encoded symbol; and

wherein the Barker encoded and CCK encoded symbols are modulated in compliance with IEEE Standard 802.11b (1999).

72. (Currently Amended) A computer program product, comprising computer readable program code causing an information processor to perform the following steps, comprising:

receiving a modulated signal including a plurality of symbols including a Barker encoded symbol defined by a first number of chips;

generating a decoded waveform upon receipt of a second number of chips less than the first number of chips of the Barker encoded symbol and before at least one of receiving, decoding, and deciding the first number of chips of the Barker encoded symbol; and

equalizing the modulated signal using the decoded waveform.

73. (Original) The product of Claim 72, wherein the modulated signal further includes a non-Barker encoded symbol defined by a second number of chips.

74. (Original) The product of Claim 73, wherein the non-Barker encode symbol comprises a CCK encoded symbol; and

wherein the Barker encoded and CCK encoded symbols are modulated in compliance with IEEE Standard 802.11b (1999).

75. (Currently Amended) An information processing system including an information processor coupled to memory, the memory comprising computer readable program code causing the information processor to perform the following operations, comprising:

receiving a modulated signal including a plurality of symbols including a Barker encoded symbol defined by a first number of chips;

generating a decoded waveform upon receipt of a second number of chips less than the first number of chips of the Barker encoded symbol and before at least one of receiving, decoding, and deciding the first number of chips of the Barker encoded symbol; and

equalizing the modulated signal using the decoded waveform.

76. (Original) The system of Claim 75, wherein the modulated signal further includes a non-Barker encoded symbol defined by a second number of chips.

77. (Original) The system of Claim 76, wherein the non-Barker encode symbol comprises a CCK encoded symbol; and

wherein the Barker encoded and CCK encoded symbols are modulated in compliance with IEEE Standard 802.11b (1999).

78. (Currently Amended) A decoding unit, comprising:

a decision feedback equalizer having an input capable of receiving modulated signal including a received symbol defined by a first number of chips and an output;

a demodulation unit coupled to the output of said decision feedback equalizer, comprising:

a decoder capable of decoding the received symbol upon receipt of the first number of chips defining the received symbol; and

partial correlation logic ~~capable of~~ for generating a decoded subsymbol upon receipt of a second number of chips of the received symbol and before at least one of receiving, decoding, and deciding the first number of chips of the received symbol, the second number being less than the ~~fast~~ first number; and

a remodulation unit coupled to said partial correlation logic of said demodulation unit and said decision feedback equalizer, said remodulation unit ~~capable of~~ for generating a subsymbol waveform corresponding to the decoded subsymbol, said decision feedback equalizer to equalize the ~~modulated~~ modulated remodulated signal using the subsymbol waveform.

79. (Original) The decoding unit of Claim 78, wherein the subsymbol waveform includes a third number of chips corresponding to the subsymbol waveform, the third number being less than or equal to the second number; and wherein said partial correlation logic generates the decoded subsymbol using correlation processing based on the second number of chips.

80. (Original) The decoding unit of Claim 78, said decision feedback equalizer comprising:

a hard decision unit coupled to said equalizer input for determining hard decision information associated with the modulated signal; and

a feedback filter coupled to said hard decision unit and said remodulation unit for equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

81. (Previously Presented) The decoding unit of Claim 78, wherein said decoder of said demodulation unit comprise first and second demodulator units capable of decoding the received symbol by at least one of first and second distinct modulation modes.

82. (Original) The decoding unit of Claim 81, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying compliant with IEEE Standard 802.11b (1999).

83. (Currently Amended) A decoder, comprising:

means for receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips; and

means for generating a subsymbol waveform upon receipt of a second number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the first symbol, and ~~provide~~ for providing the

subsymbol waveform to the receiving means, the second number being less than the first number, said receiving means including means for equalizing the modulated signal using the subsymbol waveform.

84. (Original) The decoder of Claim 83, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

85. (Original) The decoder of Claim 83, said equalizing means comprising:

hard decision means for determining hard decision information associated with the modulated signal; and

filtering means for selectively equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

86. (Original) The decoder of Claim 83, wherein said generating means comprises:

demodulation means for generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

remodulation means for remodulating a subsymbol waveform corresponding to the decoded subsymbol information.

87. (Currently Amended) A decoder, comprising:

means for receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips; and

means for generating a subsymbol waveform upon receipt of a second number of chips of the symbol and for providing the subsymbol waveform to the receiving means, the second number being less than the first number, said receiving means including means for equalizing the modulated signal using the subsymbol waveform, wherein said generating means comprises:

demodulation means for generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

remodulation means for remodulating a subsymbol waveform corresponding to the decoded subsymbol information,

~~The decoder of Claim 86,~~ wherein said demodulation means further comprises symbol correlator means for correlating the perceived second number of chips against a subset of valid candidate symbols to obtain a best match candidate, said demodulation means generating the decoded subsymbol information based on the best match candidate.

88. (Original) The decoder of Claim 86, wherein said demodulation means further comprises decision processing means for deciding the symbol upon receipt of the first number of chips defining the symbol.

89. (Original) The decoder of Claim 88, wherein said decision processing means comprises first and second demodulation pathway means capable of deciding the symbol by at least one of first and second distinct modulation modes.

90. (Original) The decoder of Claim 89, wherein said fast and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

91. (Original) The decoder of Claim 83, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

92. (Currently Amended) A feedback equalizer comprising:

means for receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips;

means for generating a subsymbol waveform upon receipt of a second number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the symbol, the second number being less than the first number; and

means for selectively filtering the subsymbol waveform from said modulated signal.

93. (Original) The equalizer of Claim 92, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

94. (Original) The equalizer of Claim 92, further comprising:

means for determining hard decision information associated with the modulated signal; and

means for selectively equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

95. (Original) The equalizer of Claim 92, wherein said generating means comprises:

demodulation means for generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

remodulation means for generating a subsymbol waveform corresponding to the decoded subsymbol information.

96. (Currently Amended) A feedback equalizer comprising:

means for receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips;

means for generating a subsymbol waveform upon receipt of a second number of chips of the symbol, the second number being less than the first number, wherein said generating means comprises:

demodulation means for generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

remodulation means for generating a subsymbol waveform corresponding to the decoded subsymbol information; and

means for selectively filtering the subsymbol waveform from said modulated signal,

~~The equalizer of Claim 95,~~ wherein said demodulation means further comprises means for correlating the perceived second number of chips against a subset of valid candidate symbols to obtain a best match candidate, said demodulation means generating the decoded subsymbol information based on the best match candidate.

97. (Original) The equalizer of Claim 95, wherein said demodulation means further comprises decision processing means for deciding the symbol upon receipt of the first number of chips defining the symbol.

98. (Original) The equalizer of Claim 97, wherein said decision processing means comprises first and second demodulation pathway means for deciding the symbol by at least one of first and second distinct modulation modes.

99. (Original) The equalizer of Claim 98, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

100. (Original) The equalizer of Claim 91, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

101. (Currently Amended) A transceiver, comprising:

means for receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips; and

means for generating a subsymbol waveform upon receipt of a second number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the symbol, and ~~provide~~ for providing the subsymbol waveform to the receiving means, the second number being less than the first number, said receiving means including means for equalizing the modulated signal using the subsymbol waveform.

102. (Original) The transceiver of Claim 101, wherein the subsymbol waveform includes a third number of chips, the third number being less than or equal to the second number.

103. (Original) The transceiver of Claim 101, said equalizing means comprising:

hard decision means for determining hard decision information associated with the modulated signal; and

filtering means for selectively equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

104. (Original) The transceiver of Claim 101, wherein said generating means comprises:

demodulation means for generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

remodulation means for re-modulating a subsymbol waveform corresponding to the decoded subsymbol information.

105. (Currently Amended) A transceiver, comprising:

means for receiving a modulated signal, the modulated signal including a symbol defined by a first number of chips; and

means for generating a subsymbol waveform upon receipt of a second number of chips of the symbol and for providing the subsymbol waveform to the receiving means, the second number being less than the first number, said receiving means including means for equalizing the modulated signal using the subsymbol waveform, wherein said generating means comprises:

demodulation means for generating decoded subsymbol information upon perceiving the second number of chips of the symbol; and

remodulation means for re-modulating a subsymbol waveform corresponding to the decoded subsymbol information,

~~The transceiver of Claim 104,~~ wherein said demodulation means further comprises symbol correlator means for correlating the perceived second number of chips against a subset of valid candidate symbols to obtain a best match candidate,

said demodulation means generating the decoded subsymbol information based on the best match candidate.

106. (Original) The transceiver of Claim 104, wherein said demodulation means further comprises decision processing means for deciding the symbol upon receipt of the first number of chips defining the symbol.

107. (Original) The transceiver of Claim 106, wherein said decision processing means comprises first and second demodulation pathway means capable of deciding the symbol by at least one of first and second distinct modulation modes.

108. (Original) The transceiver of Claim 107, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999) respectively.

109. (Previously Presented) The transceiver of Claim 101, wherein the symbol is modulated in accordance with one of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard 802.11b (1999).

110. (Original) The transceiver of Claim 101, further comprising RF and IF means for providing the modulated signal to said receiving means.

111. (Original) A base station comprising the transceiver of Claim 110.

112. (Original) A network card comprising the transceiver of Claim 110.

113. (Original) An information processing system, comprising the transceiver of Claim 101.

114. (Currently Amended) A decoder, comprising,

means for receiving a modulated signal, the modulated signal including a Barker encoded symbol defined by a first number of chips; and

means for generating a decided waveform upon receipt of the first number of chips of the symbol and before at least one of receiving, decoding, and deciding the first number of chips of the first symbol, and for providing ~~provide~~ the decided waveform to the receiving means, said receiving means including means for equalizing the modulated signal using the decided waveform.

115. (Original) The decoder of Claim 114, wherein the modulated signal further includes a non-Barker encoded symbol defined by a second number of chips.

116. (Original) The decoder of Claim 115, wherein the non-Barker encode symbol comprises a CCK encoded symbol; and

wherein the Barker encoded and CCK encoded symbols are modulated in compliance with IEEE Standard 802.11b (1999).

117. (Original) A transceiver, comprising the decoder of Claim 116.

118. (Original) A base station, comprising the transceiver of Claim 117.

119. (Original) A network card comprising the transceiver of Claim 117.

120. (Original) An information processing system comprising the transceiver of Claim 117.

121-123. (Cancelled)

124. (Currently Amended) A decoding unit, comprising:

decision feedback equalization means having an input capable of receiving modulated signal including a received symbol defined by a first number of chips and an output;

demodulation means comprising:

decoding means for ~~deciding~~ decoding the received symbol upon receipt of the first number of chips defining the received symbol; and

partial correlation logic means for generating a decoded subsymbol upon receipt of a second number of chips of the received symbol and before at least one of receiving, decoding, and deciding the first number of chips of the first symbol, the second number being less than the first number; and

remodulation means for generating a subsymbol waveform corresponding to the decoded subsymbol, said decision feedback equalization means including means for equalizing the modulated signal using the subsymbol waveform.

125. (Original) The decoding unit of Claim 124, wherein the subsymbol waveform includes a third number of chips corresponding to the subsymbol waveform, the third number being less than or equal to the second number; and wherein said partial correlation logic means generates the decoded subsymbol using correlation processing based on the second number of chips.

126. (Original) The decoding unit of Claim 124, said decision feedback equalization means comprising:

hard decision means for determining hard decision information associated with the modulated signal; and

feedback filter means for equalizing the modulated signal using one of the hard decision information and the subsymbol waveform.

127. (Original) The decoding unit of Claim 124, wherein said decoding means comprises first and second demodulator means for deciding the received symbol by at least one of first and second distinct modulation modes.

128. (Original) The decoding unit of Claim 127, wherein said first and second distinct modulation modes comprise Barker spreading and complementary code keying compliant with IEEE Standard 802.11b (1999).